a first transistor formed on a surface of said semiconductor substrate and including a first gate insulating film and a first gate electrode;

a second transistor formed on the surface of said semiconductor substrate and including a second gate insulating film and a second gate electrode; and

a charge storage layer included in said first gate insulating film and absent from said second gate insulating film,

wherein said first and second transistors are isolated by a trench and said charge storage layer in said first transistor is restricted from an element isolation region and exists only below said first gate electrode in an element region.

REMARKS

Favorable consideration of this application as presently amended is respectfully requested.

Claims 1-6 are presently active, Claim 1 having been amended by way of the present amendment.

In the outstanding Office Action, the drawings were objected to due for not being designated with a label such as --Prior Art--. The title was objected to for not being descriptive. Claims 1-6 were rejected under 35 U.S.C. §112, second paragraph, as being indefinite. Claim 1 was rejected under 35 U.S.C. §103(a) as being unpatentable over Ogura et al (U.S. Pat. No. 6,255,166) and Inoue (U.S. Pat. No. 5,559.048). Claims 2, 3, and 5 were rejected under 35 U.S.C. §103(a) as being unpatentable over Ogura et al and Inoue in view of Resinger (U.S. Pat. No. 6,137,718). Claim 4 was rejected under 35 U.S.C. §103(a) as being unpatentable over Ogura et al and Inoue and Resinger in view of Agarwal et al (U.S. Pat. No.

6,201,276). Claim 6 was rejected under 35 U.S.C. §103(a) as being unpatentable over Ogura et al and Inoue in view of Fang (U.S. Pat. No. 6,023,085).

Regarding the drawing objection, a Letter Requesting Drawing Change Approval is submitted herewith in which the label --PRIOR ART-- is added in red to Figures 14-21. Thus, it is respectfully submitted that the objection to the drawings has been overcome.

Regarding the objection to the title, the title has been amended to read --NONVOLATILE SEMICONDUCTOR MEMORY HAVING MONOS STRUCTURE AND METHOD OF FABRICATING THE SAME USING SHALLOW TRENCH ISOLATION--, thus providing a descriptive title of the invention. Thus, it is respectfully submitted that the objection to the title has been overcome.

Regarding the 35 U.S.C. §112, second paragraph, rejection, Claim 1 has been amended to define a memory having a charge storage layer included in a first gate insulating film of a first transistor, absent from a second gate insulating film of a second transistor, and restricted from an element isolation region of the memory. Thus, as amended, Claim 1 distinctly and particularly points out those features of the claimed invention. Hence, it is respectfully submitted that the 35 U.S.C. §112, second paragraph, rejection has been overcome.

According to the features set forth in Claim 1, the charge storage layer included in the first gate insulating film of the first transistor exists only below the first gate electrode in an element region of the memory and is restricted from an element isolation region of the memory. Applicant submits that charge retention characteristics of a memory are lowered if the charge storage layer extends into an element isolation region of the memory.

Specifically, Applicant's specification states that:

> ... the charge storage layer 112 in a gate insulating film in a memory cell is formed only on a channel region of the cell, not on an element isolation region. Therefore, the phenomenon does not occur which is a problem for the charge retention characteristics, and in which electric charge moves from a charge storage layer on the channel of a cell transistor to a charge storage layer on the element isolation region.[2]

The outstanding Office Action asserts that Claim 1 is obvious over Ogura et al and Inoue. M.P.E.P. §2143.03 requires that to establish a case of *prima facie* obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. However, neither Ogura et al nor Inoue disclose or suggest a charge storage layer existing only below the first gate electrode in an element region of a memory and restricted from an element isolation region, as defined in Claim 1.

Ogura et al depict in Figure 1 a nonvolatile memory cell having a first transistor including a first gate insulating film 132 (containing a charge storage layer 132b) and a first gate electrode 142, and a second transistor including a second gate insulating film 131 and a second gate electrode. Ogura et al do not show a first and second transistor isolated by a trench, as acknowledged in the outstanding Office Action.[3] With no structure by which to clearly delineate an element isolation region, Applicant submits that it is unclear whether the charge storage layer in Ogura et al is restricted from an element isolation region of the memory. Hence, Ogura et al, in addition to not teaching a trench structure, do not disclose or suggest a charge storage layer existing only below a first gate electrode in an element region of the memory and restricted from an element isolation region, as defined in Claim 1.

Inoue, while depicting a trench structure, depicts in Figure 9G a double layered floating gate EPROM having a floating gate 103, a floating gate 106, and a control gate 110.

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[2]Specification, page 13, lines 11-20.

[3]Office Action, page 4, lines 3-5.

If the first and second gates 103 and 106 are considered to be a charge control layer in Inoue, then electrons injected into floating gate 103, due to the electrical interconnection between the floating gates, will diffuse across the extent of the floating gate 106. As a result, the electric charge above the channel region in Inoue is reduced, thereby lowering the above-noted charge retention characteristics of the memory. Furthermore, as shown in Figure 9G of Inoue, floating gate 106 extends above the isolation trench groove 107 and the trench groove impurity region 120, both used along with the isolation trench 108 in Inoue for element isolation.[4] Thus, if the first and second gates 103 and 106 are considered to be a charge control layer in Inoue, this layer is not restricted from the element isolation region of the memory, as defined in Claim 1.

Hence, like in Ogura et al, there is no teaching or suggestion in Inoue for a charge storage layer existing only below a first gate electrode in an element region of the memory and restricted from an element isolation region, as defined in Claim 1.

M.P.E.P. §2143.03 requires to establish *prima facie* obviousness that all the claim limitations must be taught or suggested by the applied prior art. With no features disclosed or suggested in the applied prior art of Ogura et al and Inoue for the claimed charge storage layer defined in Claim 1, a case of *prima facie* obviousness has not been established.

Thus, it is respectfully submitted that Claim 1 and Claims 2-6 which depend from Claim 1 are not obvious and patentably define over the applied prior art.

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[4]Inoue, col. 9, lines 39-50.

Consequently, in view of the present amendment and in light of the above discussions, the outstanding grounds for rejection are believed to have been overcome. The application as amended herewith is believed to be in condition for formal allowance. An early and favorable action to that effect is respectfully requested.

Respectfully submitted,

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Amendment Filed on: _____

IN THE TITLE

Please amend the title as follows:

NONVOLATILE SEMICONDUCTOR MEMORY HAVING MONOS STRUCTURE AND METHOD OF FABRICATING THE SAME USING SHALLOW TRENCH ISOLATION

IN THE CLAIMS

Please amend Claim 1 as shown below:

1. (Amended) A nonvolatile semiconductor memory comprising:

a semiconductor substrate;

a first transistor formed on a surface of said semiconductor substrate and including a first gate insulating film and a first gate electrode; [and]

a second transistor formed on the surface of said semiconductor substrate and including a second gate insulating film and a second gate electrode[,]; and

a charge storage layer included in [wherein] said first gate insulating film [includes a charge storage layer] and absent from said second gate insulating film [does not include a charge storage layer],[and]

wherein said first and second transistors are isolated by a trench and said charge storage layer in said first transistor [does not exist in] is restricted from an element isolation region and exists only below said first gate electrode in an element region.